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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,217	02/19/2004	Kevin Nolish	FORE-107	5328

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Ansel M. Schwartz
Attorney at Law
Suite 304
201 N. Craig Street
Pittsburgh, PA 15213

EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,217	NOLISH ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 4/16/07
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on April 16, 2007 for the application of Nolish et al., for a "Method, apparatus and software for preventing switch failures in the presence of faults" filed February 19, 2004.

Information disclosed and listed on PTO 1449 has been considered.

Claims 1-8, and 10-19 are pending in the application.

Claims 8, and 10-19 are rejected under 35 U.S.C. 101

Claims 1-5 are rejected under 35 USC § 102.

Claims 6-8, and 10-19 are rejected under 35 USC § 103.

Claims 8, 10, and 17 have been amended.

Claim Objections

In view of the Applicant's amendments, the previous claim objections have been withdrawn.

Claim Rejections - 35 USC § 101

Claims 8, and 10-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Examiner would like to point out that a program has to be stored on a computer-readable medium. The Examiner suggests amending claim 8 to include the limitation of "A software program stored on a computer-readable medium".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Abramson (U.S. Patent No. 6,000,043).

As per claim 1, Abramson discloses a switch for transferring data (Fig. 2) comprising:

at least one master unit (Fig. 2, element 43a) a plurality of slave units (Fig. 2, elements 40a-b and 50a-c) a bus through which the master unit communicates with the slave units (Fig. 2, element 45)

and a memory (Fig. 2, element 35) in communication with the master unit having a software program that causes the master unit to automatically recover (col. 3, lines 20-26) when a slave unit fails (Fig. 6a, elements 111a-b) which has caused the master unit to fail (Fig. 6a, element 103, *master abort*) and (col. 7, lines 44-47).

As per claim 2, Abramson discloses persistent storage (Fig. 2, element 35) that survives across abnormal termination of the master unit (Fig. 6a, element 103, *master abort*).

As per claim 3, Abramson discloses a mechanism for detecting failures of the slave units (Fig. 6b, elements 111a-b) and (col. 7, lines 44-47) and thereupon causes the master unit to abnormally terminate (Fig. 6a, element 103, *master abort*).

As per claim 4, Abramson discloses the software program causes the master unit to automatically recover when the detecting mechanism causes the master unit to abnormally terminate (col. 3, lines 20-26).

As per claim 5, Abramson discloses detecting mechanism includes a hardware watchdog device (col. 6, lines 20-27, expiration of timer).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6-8, and 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramson (U.S. Patent No. 6,000,043) in view of Cepulis et al. (U.S. Patent No. 6,463,550).

As per claim 6, Abramson discloses a method for transferring data comprising the steps of:

attempting to access a failed slave unit of a plurality of slave units (Fig. 2, elements 40a-b and 50a-c) of a switch by a master unit (col. 7, lines 44-47) of the switch with a signal through a bus through which the master unit (Fig. 2, element 43a) and the failed slave unit communicate (Fig. 2, element 45)

and automatically recovering (col. 3, lines 20-26) the master unit, which has failed (Fig. 6a, element 103, *master abort*) and (col. 7, lines 44-47) because the failed slave unit failed (Fig. 6b, elements 111a-b) with a software program in the switch (col. 3, lines 20-26).

Abramson fails to explicitly disclose avoiding access to the failed device. Cepulis teaches:

that directs the master unit to avoid further accessing (col. 5, lines 21-34, *prevent access*) the failed slave unit of the plurality of slayer units (Fig. 5, element 508, *tag failed device*).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of management of peripheral devices of Abramson in combination with the fault detection and isolation system of Cepulis et al. to effectively detect system failures.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Abramson discloses a method of identifying a faulty peripheral device by its address (col. 3, lines 17-19) and Cepulis et al. uses a method of assigning addresses to physical devices to identify a faulty device (col. 5, lines 29-34). Assigning logical addresses to physical devices permits efficient use of the computer's physical resources by the operating system and applications software (Cepulis, col. 2, lines 22-24).

As per claim 7, Abramson discloses a method as described in claim 6 wherein the recovering step includes the step of obtaining status information about the slave units from persistent storage (col. 3, lines 20-26, *status register*).

As per claim 8, Abramson discloses a software program whose contents causes a processor to perform the steps of:

Determining a master unit abnormally terminated when the master unit (Fig. 6a, element 103, *master abort*) attempted to access a first slave unit (col. 7, lines 44-47) identifying the first slave unit of a plurality of slave units of a switch has failed (Fig. 6b, elements 111a-b) when the first slave unit is attempted to be accessed by the master unit of the switch (col. 7, lines 44-47)

Cepulis teaches:

and preventing a master unit from attempting to access (col. 5, lines 21-34, *prevent access*) the failed first slave unit (Fig. 5, element 508, *tag failed device*).

As per claim 10, Cepulis discloses the step of changing information in persistent storage associated with the first slave unit from identified as failed to identified as good if the master unit does not terminate abnormally after the master unit attempts to contact the slave unit (col. 12, lines 62-67 through col. 13, lines 1-2).

As per claim 11, Cepulis discloses the step of setting a variable slot chosen from amongst a plurality of slots of the switch not marked as potentially bad (col. 5, lines 14-20, failed device log) and (Fig. 5, element 508, tag failed devices).

As per claim 12, Cepulis discloses the step of determining whether the first slave unit is physically present in a first slot of the plurality of slots (col. 8, lines 3-9).

As per claim 13, Cepulis discloses the step of determining the first slot is marked to be skipped (col. 5, lines 14-20, failed device log) and (Fig. 5, element 508, tag failed devices).

As per claim 14, Cepulis discloses the step of marking the variable slot as potentially bad if it is not marked potentially bad (col. 5, lines 14-20, failed device log) and (Fig. 5, element 508, tag failed devices).

As per claim 15, Cepulis discloses the step of reporting the variable slot as containing broken hardware (col. 5, lines 14-20, failed device log) and preventing the

master unit from attempting to access the variable slot (col. 5, lines 21-34, *prevent access*) if the variable slot is marked to be skipped and (Fig. 5, element 508, tag failed devices).

As per claim 16, Cepulis discloses the step of attempting to access hardware present in the variable slot if the variable slot is marked potentially bad (col. 5, lines 14-20, failed device log) and (Fig. 5, element 508, tag failed devices).

As per claim 17, Cepulis discloses the step of marking the variable slot as good if the switch did not abnormally terminate when the master unit accessed the first slave unit (col. 12, lines 62-67 through col. 13, lines 1-2).

As per claim 18, Cepulis discloses the step of enabling normal operations on hardware present in the variable slot if the variable slot is marked as good (col. 12, lines 62-67 through col. 13, lines 1-2).

As per claim 19, Cepulis discloses the step of setting the variable slot to a next slot of the plurality of slots (Fig. 5, element 516, *check for remaining devices*).

Response to Arguments

Applicant's arguments filed April 16, 2007, with respect to claims 1-8, and 10-19 have been fully considered but they are not persuasive.

As per claims 1 and 6, in response to applicant's arguments that Abramson fails to disclose the master unit to automatically recover when a slave unit fails which has caused the master unit to fail, the Examiner respectfully disagrees and would like to point out to column 5, lines 55-59, wherein Abramson discloses in a DDMA system or otherwise, if the peripheral target device will not respond (i.e., it will not claim the transaction by failing to assert the DEVSEL# signal), the bridge circuit 33 (or the bus master in question) will perform an abort, such as a Master Abort in a PCI architecture. Abramson discloses when one of the slave devices fails to respond (i.e. slave unit fails), it causes a Master abort (i.e. master bus terminating abnormally due to the failed slave unit).

Figures 6a and 6b show the process of determining which slave device caused the Master abort. Column 8, lines 11-18, wherein Abramson discloses if the CPU identifies the cause of the Master Abort condition (decision block 116), control passes to blocks 117 and 118 where the operation of the SMM code interacts with the Operating System (O/S) by passing the information as to cause and improperly operating peripheral device. The operation of the O/S system then attempts to correct the problem by itself or with the assistance of the user (i.e. automatically recover).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER